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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,178	07/25/2000	Hiroki Nakamura	F98ED0762	7254

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EXAMINER	
MAI, ANH D	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 06/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,178	NAKAMURA, HIROKI	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *21-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 March 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Amendment

Amendment filed March 28, 2002 is entered as Paper No. 11. Claims 1, 3-5, 10, 11, 13-16, 19 and 20 have been amended. Claims 27-33 have been added.

Drawings

1. The corrected or substitute drawings were received on April 03, 2002. These drawings are acceptable.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following suggestion is more descriptive : SEMICONDUCTOR DEVICE HAVING WIRING PATTERNS AND DUMMY PATTERNS COVERED WITH INSULATING LAYER.

Response to Amendment

3. The amendment filed March 28, 2002 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: **wherein the edge of the insulating layer is located on the pad pattern which is adjacent to the dummy pattern**. (shown in claim 29, the last 2 lines).

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 29-33 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "**wherein the edge of the insulating layer is located on the pad pattern which is adjacent to the dummy pattern**" in the application as filed.

The insulating layer that is not formed over the dummy pattern is the second insulating layer 606. (See instant Fig. 7A).

The second insulating layer 606 has not formed on the pad pattern. Therefore, the claimed matter: edge of the insulating layer is located on the pad pattern is new and doe not have support in the originally filed application.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 11 and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites: a **third** dummy pattern formed **between** the first dummy pattern and the wiring pattern, the first insulating layer being not formed on the third dummy pattern.

As shown in Fig. 6, the third dummy pattern appears to be dummy pattern 500a (formed between the first dummy pattern 500b and the wiring pattern 500).

However, the first insulating layer 502 clearly formed on the third dummy pattern 500a as well as all of the metal 500's.

With respect to claim 16, limitations of the claim includes: a fourth pattern surrounding the bonding pad, on line 4. One pattern (fourth) can not surround any thing.

6. Claims 16-20 and 29-33 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 16-20 and 29-33 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in Paper No. 11 filed March 28, 2002. In that paper, applicant has stated the circuit are, wiring pattern, is separated from the peripheral area, dummy patterns, and this statement indicates that the invention is different from what is defined in the claim(s) because Fig. 7A, shows the pad 601 is formed between the dummy patterns 600a and 600b, which is in the peripheral area not in the circuit area as claimed.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,789,313) in view of Hosoda et al. (JP-08-181208).

Lee teaches a semiconductor device substantially similar as claimed including:

a semiconductor substrate (10) having a circuit area where an integrated circuit is formed and a peripheral area surrounding the circuit area;

wiring patterns (20) formed on the substrate in the circuit area;

a first dummy pattern (42/22) which is formed of the same material as the wiring pattern, formed in the peripheral area;

a first insulating layer (46) formed on an circuit area and the peripheral area of the semiconductor substrate (10);

a second insulating layer (48) formed on the first insulating layer which is formed on the semiconductor substrate, wherein the second insulating layer is not formed over the first dummy pattern (42); and

a third insulating layer (50) formed on the exposed first insulating layer (46) and the second insulating layer (48). (See Fig. 7D).

Thus, Lee is shown to teach all the features of the claim with the exception of explicitly show that the dummy pattern encompassing the circuit area.

However, Hosoda teaches that the dummy patterns (14a) can be formed any where on a chip including surrounding the circuit pattern, hence peripheral (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the dummy patterns (42) of Lee surrounding the circuit patterns (20) as taught by Hosoda to improve the planarity of the chip.

Regarding the circuit area and the peripheral area, it is well known that all semiconductor chip has circuit area where the IC is formed and the peripheral area surrounding the circuit.

Product by process limitation:

The expression "the width of the first (and third) dummy pattern is fixed by a concentration of solid content of the SOG (claims 3, 14 and 19); where a concentration of solid content of the SOG layer is around 5.2 wt% (claims 4, 10, 15 and 20); thermally planarized surface (claim 5)" are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that, the solid content of the SOG only is only **existed before** being deposited on the semiconductor substrate, as a semiconductor device, the SOG layer is **no longer contained 5.2 wt %** as claimed.

With respect to claim 2, the second insulating layer (48) of Lee is a SOG layer.

With respect to claim 3, the first dummy pattern (42) of Lee has a width, which appears to be fixed by a concentration of solid content of the SOG. (product-by-process).

With respect to claim 4, the width of the first dummy pattern (42) of Lee is designed for various size including less than 1μm. Additionally, since the SOG (48) is formed in the spaces between the metal lines of Lee, thus, it also encompass the claimed limitation.

With respect to claim 5, the semiconductor device of Lee also includes multi-layered wiring; wherein the dummy pattern can be formed on the first and second level of a three levels wiring.

Thus, the semiconductor device of Yamaha is substantially similar as claimed including:

a second dummy pattern (44) formed under the first dummy pattern (44); and

a fourth insulating layer (18) formed directly on the substrate (10) and on the second dummy pattern (44), the fourth insulating layer (18) including a planarized surface, whereby, the first dummy pattern (44) is formed the fourth insulating layer (18) which is formed on the second dummy pattern (44), and the wiring patterns (20) are formed on the fourth insulating layer (18). (See Fig. 12).

With respect to claim 6, the shape and size of the second dummy pattern (44) of Lee appears to be almost the same as these of the first dummy pattern (44).

With respect to claim 7, the fourth insulating layer (18) of Lee is BPSG layer.

With respect to claim 8, the second insulating layer (48) of Lee is a SOG layer.

With respect to claim 9, the width of the first and second dummy patterns (44) of Lee appears to be fixed by a concentration of solid content of the SOG.

With respect to claim 10, the each of the width of the first and second dummy patterns (44) of Lee has a width, which is designed for various size including less than 1μm.

Additionally, since the SOG (48) is formed in the spaces between the lines (12) of Lee, thus, it also encompass the claimed limitation.

With respect to claim 11, as best understood by the examiner, the semiconductor device of Lee further includes:

a third dummy pattern (44) formed between the first dummy pattern (44) and the wiring pattern (20), the first insulating layer (46) being formed on the third dummy pattern (44).

The peripheral area has been discussed above.

With respect to claim 12, the width of the third dummy pattern (44) is almost the same as that of the first dummy pattern (44).

With respect to claim 13, there is a distance between the first and third dummy patterns of Lee. Lee further teaches that the width of the line will approximately equal the spacing of the lines in areas where lines are closely spaced. Since the dummy lines of Lee are formed to be 1μm or less, thus, the spacing of the first and third dummy lines of Lee is within the claimed range.

Further, the claimed value of "over 0.9μm" does not appear to be critical.

Therefore, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum spacing of the dummy lines. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

With respect to claim 14, the each of the first and third dummy patterns (44) of Lee has a width, which appears to be fixed by a concentration of solid content of the SOG.

With respect to claim 15, the each of the first and third dummy patterns (44) of Lee has a width, which is designed for less than 1μm. The concentration of solid content of the SOG has been discussed above.

8. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee '313 and Hosoda as applied to claim 1 above, and further in view of Yang et al. (U.S. Patent No. 5,798,298).

With respect to claim 16, Yamaha and Hosoda teach all the features of the claim with the exception of a boding pad formed on the semiconductor substrate .

However, Yang teaches a semiconductor device including:

a bonding pad (30) formed on the semiconductor substrate (3) in the circuit area;

a fourth dummy pattern (34) surrounding the bonding pad. (See Fig. 3C).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the semiconductor device of Lee having a bonding pad (30) formed between the dummy pattern as taught by Yang to making contact to the other devices.

With respect to "the second insulating layer being not formed on the fourth dummy pattern", the second insulating layer (48) of Lee is not formed on the metal lines, thus, the fourth dummy pattern (44) is included.

With respect to claim 17, the width of the fourth dummy pattern (34) of Yang (or Lee) appears to be almost the same as that of the first dummy pattern (34).

With respect to claim 18, the spacing of the dummy pattern has been discussed above.

With respect to claims 19 and 20, similar matters have been discussed above.

9. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha et al. (JP-10-270445) in view of Hosoda et al. (JP-08-181208).

Yamaha teaches a semiconductor device substantially similar as claimed including:

a semiconductor substrate (10) having a circuit area where an integrated circuit is formed and a peripheral area surrounding the circuit area;

wiring patterns (12s) formed on the substrate (10) in the circuit area (RA);

a dummy pattern (13) which is formed of the same material as the wiring pattern (12), formed in the peripheral area (RB), the dummy pattern encompassing the circuit area (RA); and a insulating layer (14b) formed above the semiconductor substrate (10), the insulating layer being formed outside the dummy pattern but no being formed over the dummy pattern, and the insulating layer having a moisture absorbable characteristic. (See Fig. 5).

Thus, Yamaha is shown to teach all the features of the claim with the exception of explicitly show that the dummy pattern surrounding the circuit area.

However, Hosoda teaches that the dummy patterns (14a) can be formed any where on a chip including surrounding the circuit pattern at the edge of the chip.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the dummy patterns (13) of Yamaha surrounding the circuit patterns (12s) as taught by Hosoda to improve the planarity of the semiconductor device.

Regarding the moisture absorbable characteristic, since the insulating layer (14b) of Yamaha is SOG, thus, the insulating layer (14b) of Yamaha has a moisture absorbable characteristic as claimed.

With respect to claim 28, the insulating layer (14b) of Yamaha is a second layer, the semiconductor device of Yamaha further comprises first (14a) and third (14c) insulating layers formed on the substrate, the second insulating layer (14a) being located between the first insulating layer (14a) and the third insulating layer (14c).

Response to Arguments

10. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

11. With respect to claims 29-33, since the claimed subject matters are new and unsupported by the originally filed application, the Action on merit of these claims are not warranted.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
June 6, 2002

OLIK CHAUDHURI
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